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A Survey on Energy Efficient Multicore and Multiprocessor Systems in IOT: Architecture, Thread Scheduling and Communication

EE5902 CA Report

***Abstract –* In this project, we explored six papers which aim to achieve energy efficiency in multicore and multiprocessor systems in the field of IoT** applications. In “A Hierarchical Reconfigurable Micro-coded Multi-core Processor for IoT Applications[1]**”, the author proposed a simplified logic and shallow pipelined reconfigurable multi-core architecture which utilize long microinstructions for better energy efficiency. In “**ECAP: Energy Efficient CAching for Prefetch Blocks in Tiled Chip MultiProcessors[2]**”, the author explore the technique of using nearby chip free cache set as virtual cache and Confidence-Aware Replacement policy (CARP) to avoid extra energy consumption for unnecessary memory fetching. In “**Energy-Efficient Hardware-Accelerated Synchronization for Shared-L1-Memory Multiprocessor Clusters[3]**”, the author introduced a light-weight hardware-supported synchronization solution to reduce the synchronization overhead in terms of cycles and energy.**

# INTRODUCTION

# PATHS TO ENERGY EFFICIENCY

# DETAIL IMPLEMENTATIONS

# IMPLEMENTATION METHOD COMPARISONS

## Architecture

## Network communication

## Memory caching, distribution, and access

## Task mapping

## Security and reliability

# PERFORMANCE QUANTIFICATIONS AND RESULTS COMPARISONS

# UNIQUNESS IN THE IMPLEMENTATIONS